REMARKS

The Office Action of July 13, 2007, has been carefully considered and these remarks are responsive thereto. No amendments have been made. Claims 59-72 and 74-82 remain pending. Reconsideration and allowance are respectfully requested.

Rejection Under 35 U.S.C. § 102 based on IBM Technical Disclosure

Claims 59-72 and 74-82 stand rejected under 35 U.S.C. § 102(a) as being anticipated by IBM Technical Disclosure,[1] hereinafter IBM. Applicant respectfully traverses.

In order to preserve its rights, Applicant maintains and resubmits its previous arguments from the Response filed April 6, 2007. Those arguments immediately follow. However, Applicant provides additional remarks thereafter, in an effort to clarify the reasoning therein.

Arguments from April 6, 2007, Response

The Primary Examiner alleged that the "IBM document discloses interconnected programmable chips on a substrate which are connected to and configured by another chip or part of a chip." (See Office Action, page 2, lines 26-28.) Assignee respectfully submits that the Primary Examiner's assertion is not entirely correct. As illustrated in Figure 1, the chips 2 are connected by wiring line segments 3 formed on a "silicon wiring wafer 1…used as a carrier for chips 2 and as a chip interconnection means." (See the IBM Technical Disclosure, lines 1 and 2.) Thus, the IBM Technical Disclosure appears to teach something akin to a configurable printed circuit board, not an interconnect chip. Contrary to the Primary Examiner's suggestion, nothing in the IBM Technical Disclosure would teach or suggest that a chip 2 (or part of a chip 2) mounted on the wafer 1 interconnects any other chips 2 together. At most, the IBM Technical Disclosure teaches that a chip 2 could be used to control the interconnection function of the wafer 1.

Claims 59-66 and 74-76 recite

> …at least one programmable integrated circuit mounted on the at least one second region and containing a plurality of conductive leads, the at least one programmable integrated circuit being programmable by a user to at least partially form an interconnect of selected electrically conductive traces on the printed circuit board to achieve a desired electrical function from the electronic components…

Similarly, claims 67-70 and 77-79 recite

[1] It is Applicants' understanding that the Examiner is referring to the IBM Technical Disclosure entitled "Logically Controlled Chip Interconnection Technique."

> ...at least one programmable integrated circuit chip mounted on the printed circuit board, selected ones of the second electrical contacts receiving leads from the at least one programmable integrated circuit chip thereby to enable a user to programmably at least partially form an interconnect of selected ones of the first electrical contacts so as to configure the electronic components to be mounted on the printed circuit board into a selected electrical circuit...

while claims 71, 72, and 80-82 then recite

> ...one or more programmable interconnect chips mounted on the printed circuit board, selected ones of the PIC holes receiving leads from the one or more programmable interconnect chips to enable a user to programmably at least partially form an interconnect of the electronic components into a desired electrical circuit...

Accordingly, Assignee respectfully submits that the IBM Technical Disclosure would not teach or suggest these features of the invention recited in claims 59-72 and 74-82. Assignee instead points out that the IBM Technical Disclosure would, in fact, teach away from these features of the invention. Assignee therefore asks that the rejection of claims 59-72 and 74-82 over the IBM Technical Disclosure be withdrawn.

Clarifying Remarks

The technique described in IBM is used to interconnect *chips* 2 located at chip sites 7. The present claims, however, interconnect electrically conductive traces of the printed circuit board that in turn are connected to component contacts. In addition, each claim indicates that the printed circuit board has in at least one first region a plurality of component contacts configured to receive electronic components. IBM is completely devoid of this aspect of the claims. Insofar as the Office might argue that the chips 2 *are* the electronic components, the Office should take note that the claims separately and distinctly recite at least one programmable integrated circuit mounted on the at least one second region and containing *a plurality of conductive leads*, as quoted in Applicant's previous arguments. That is, the electronic components are claimed as separate and distinct from any programmable integrated circuit mounted on the circuit board. The claims require *component contacts* connected to *conductive leads* via *electronic traces*. Thus, the chips 2 in IBM cannot be both the electronic components for purposes of satisfying the claim feature "plurality of component contacts configured to receive electronic components," at the same time as being a "programmable integrated circuit." Stated another way, IBM does not teach or suggest "an electrically conductive path from each of the *component contacts* to the corresponding *conductive lead* of the at least one programmable integrated circuit," as claimed.

In addition to the above, each independent claim recites the structural formation of the apparatus as being in a "standard formation." For example, claim recites "a standard configuration independent of the electronic components and the electrical function to be implemented by the electronic components when selectively interconnected by the at least one programmable integrated circuit," whereas claims 67 and 71 each recite "a standard configuration independent of the electronic components to be mounted on the printed circuit board." IBM lacks any such standard configuration. Indeed, IBM actually *teaches away* from using a standard configuration, stating that "[p]ersonalization of the interconnection is determined by the specific system interconnection or configuration requirements...." IBM, p. 1, second full paragraph.

In sum, the IBM document does not anticipate any of the claims at least because:

- IBM lacks component contacts configured to receive electronic components, as claimed;
- IBM lacks an electrically conductive path from each of the *component contacts* to the corresponding *conductive lead* of the at least one programmable integrated circuit, as claimed; and
- IBM lacks, and even *teaches away* from, using a standard configuration, as claimed.

Applicant therefore respectfully requests the rejection over IBM be withdrawn.

Rejection Under 35 U.S.C. § 102 based on Carter

Claims 59-72 and 74-82 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 4,706,216, hereinafter Carter. Applicant respectfully traverses.

The Office Action indicates that Applicant's argument/distinction is not understood. For clarity, Applicant reproduces below the arguments set for in its April 6, 2007, Response, followed by clarifying remarks.

Arguments from April 6, 2007, Response

The Carter patent is directed to a configurable logic element. The Carter patent does not, however, teach or suggest using this element to interconnect a plurality of electrically conductive traces formed on a printed circuit board, as recited in 59-72 and 74-82. Instead, to the extent that the logic element of the Carter patent might be used with a printed circuit board,[2] the purpose of

[2] Assignee respectfully points out that the Carter patent does not, in fact, appear to even mention a printed circuit board.

the Carter logic element would seem to be to insert some type of logical operation (e.g., an AND operation, an OR operation, a NOR operation, etc.) between electrically conductive traces, rather than simply connecting them as recited in claims 59-72 and 74-82.

Assignee therefore submits that the Carter patent would not teach or suggest the features of the invention recited in any of claims 59-72 and 74-82. It is thus requested that the rejection of these claims based upon the Carter patent be withdrawn.

Clarifying Remarks

As is succinctly stated above, Carter does not teach or suggest "the at least one programmable integrated circuit being programmable by a user to at least partially form an *interconnect* of selected electrically conductive traces *on the printed circuit board* to achieve a desired electrical function *from the electronic components*," as recited in claim 59 (emphasis added). That is, Carter, at best, describes configurable logic elements that, by Carter's own admission, refer to a combination of devices which are capable of being electrically interconnected by switches operated in response to control bits stored on the chip (or transmitted to the chip) to perform any one of a plurality of *logical* functions. Carter, col. 1, lines 31-36 (emphasis added). Carter does not teach or suggest that a logic element may even be used as a programmable interconnect chip, much less that a logic element is programmable by a user to at least partially form an *interconnect* of selected electrically conductive traces *on the printed circuit board* to achieve a desired electrical function *from the electronic components*, as recited in claim 59. Claims 67 and 71 recite similar features and are allowable for similar reasons.

Applicant therefore respectfully requests the rejection over Carter be withdrawn.

CONCLUSION

All issues having been addressed, Applicant respectfully submits that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same. However, if for any reason the Examiner believes the application is not in condition for allowance or there are any questions, the Examiner is requested to contact the undersigned at (202) 824-3153.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated this 13th day of Nov., 2007

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